4521B

24-STAGE BINARY COUNTER

GENERAL DESCRIPTION — The 4521B is a timing circuit consisting of an on-chip oscillator circuit and a 24-stage binary ripple counter. The device has two Oscillator Inputs (I_1 and I_2) and two Oscillator Outputs (O_1 and O_2), Source Connections to the n-channel and p-channel transistors of the oscillator circuit (S_N and S_P), a Master Reset Input (MR) and Data Outputs from the last seven stages of the 24-stage Ripple Counter (Q_{17}-Q_{23}).

The 4521B, as shown in the Block Diagram, may be used with either an external crystal oscillator circuit, an external RC oscillator circuit, or external clock input. Oscillator Output, O_2, is available for driving additional external loads. The oscillator circuit may be made less sensitive to variations in the power supply voltage by adding external resistors R_1 and R_2 (See Block Diagram). If these external resistors are not required, Source Connection S_P must be tied to V_{DD} and Source Connection S_N must be tied to V_{SS}.

The 24-Stage Ripple Counter advances on the HIGH-to-LOW transition of the clock input with parallel Data Outputs (Q_{17}-Q_{23}) from the last seven stages available.

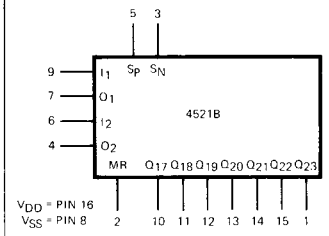
A HIGH on the Master Reset Input (MR) clears all counter stages, forcing all Parallel Data Outputs (Q_{17}-Q_{23}) LOW and disables the oscillator circuit, independent of all other inputs. This allows for very low standby power dissipation.

- **ON-CHIP CRYSTAL OSCILLATOR CIRCUIT OR ON-CHIP RC OSCILLATOR CIRCUIT OR EXTERNAL CLOCK INPUT**
- **MASTER RESET INPUT CLEARS ALL COUNTER STAGES AND DISABLES OSCILLATOR CIRCUIT FOR LOW STANDBY POWER**
- **EXTERNAL SOURCE CONNECTIONS FOR IMPROVED TIMING STABILITY**
- **OSCILLATOR OUTPUT AVAILABLE FOR DRIVING EXTERNAL LOADS**
- **MASTER RESET INPUT FACILITATES DIAGNOSTICS**

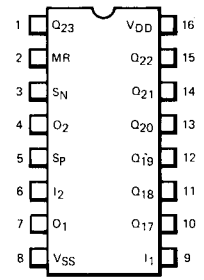
PIN NAMES

I_1, I_2	Oscillator Inputs
S_P	Source Connection-to-p-channel transistor
S_N	Source Connection-to-n-channel transistor
MR	Master Reset Input
O_1, O_2	Oscillator Outputs
Q_{17}-Q_{23}	Data Outputs

LOGIC SYMBOL

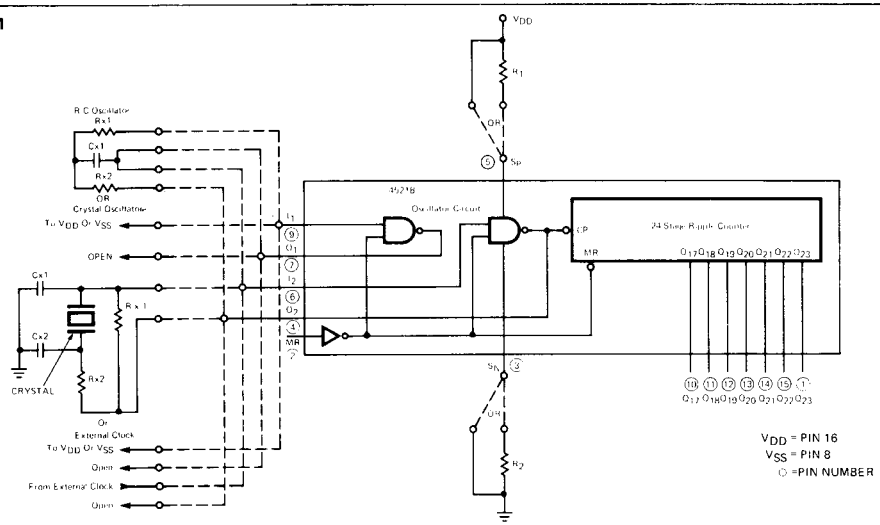


CONNECTION DIAGRAM
DIP (TOP View)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

BLOCK DIAGRAM



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